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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,971	10/30/2003	Giovanni Naso	400.210US01	8500
27073	7590	03/03/2006	EXAMINER	
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			KERVEROS, JAMES C	
			ART UNIT	PAPER NUMBER
			2138	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/696,971	Applicant(s) NASO, GIOVANNI
	Examiner JAMES C. KERVEROS	Art Unit 2138

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 30 October 2003.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-26 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) 14-17 and 22 is/are allowed.

6)  Claim(s) 1-8, 12, 13, 18-21 and 23-26 is/are rejected.

7)  Claim(s) 9-11 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 30 October 2003 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/4/04.  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_.

## DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed 10/30/2003. Claims 1-26 are pending and presently under examination.

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), ITALY RM2003A000040 filed 01/31/2003. The certified copy has been filed in parent Application No. 10/696971 filed on 10/30/2003.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8, 12, 13, 18, 19, 20, 21, 23-26 are rejected under 35 U.S.C. 103(a) as being obvious over Roohparvar et al. (U.S. Patent No. 6,016,561) ISSUED: January 18, 2000 in view of Manning (U.S. Patent No. 6,032,274) ISSUED: February 29, 2000.

Regarding Claims 1-5, 7, 8, 18, 19, 20, 23, 24, Roohparvar discloses an output data compression apparatus and method, such as a pattern recognition block 40 in memory chips 24, 26, 28, 30, which receives the data sendat[15:0] from the sense amplifiers 34 and compress that data down to 4 bit, Figures 2, 4, 5, comprising:

a first circuit and a second circuit corresponding to detection block 48 in the pattern recognition block 40 for detecting patterns all "0" or all "1"; among the data bits sendat[15:0], i.e., detect patterns in which the data bits sendat[15:0] are arranged. Specifically, the purpose of the detection block 48 is to detect when the data lines sendat[15:0] are either all "0" or all "1". When either all "0" or all "1" is detected, the MATCH output goes to "1"; otherwise, the MATCH output remains at "0". The output logic 52 receives the MATCH output and generates a number of output data bits CMPOUT [15:0], Figure 5.

Roohparvar does not explicitly disclose "an output buffer circuit that either passes the predetermined bit or is in a high impedance state in response to the first or second match signals". In analogous art, Manning discloses a buffer driver circuit 128, Figure 2, where if data read from a location in the banks 80a-80h does not match the data written to the location, the driver circuit 128 is driven to a tri-state condition. In the tri-state condition, the driver circuit 128 presents high impedance, floating output to the data bus 130. A test head 111 indicates the tri-state condition to test circuitry 113 that identify the erroneous data. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the output logic 52 of Roohparvar by incorporating a buffer driver circuit, which presents a high impedance, floating output to the data bus in response to a MATCH output signal as taught by Manning, so as to identify the erroneous data to a test circuitry.

Regarding Claim 6, Roohparvar discloses the memory device is a flash memory device, as described accordingly, "four data pins were chosen because certain flash

memory chips, such as the memory chips 24, 26, 28, 30, require at least 4 I/O pins to pass the basic write commands, such as for example, program, erase, erase suspend and status read".

Regarding Claims 12, 13, Roohparvar discloses an output data compression apparatus, such as a pattern recognition block 40 in a flash memory chips 24, 26, 28, 30, which receives the data  $sendat[15:0]$  from the sense amplifiers 34 and compress that data down to 4 bit, Figures 2, 4, 5, comprising:

a first circuit and a second circuit corresponding to detection block 48 in the pattern recognition block 40 for detecting patterns all "0" or all "1"; among the data bits  $sendat[15:0]$ , i.e., detect patterns in which the data bits  $sendat[15:0]$  are arranged. Specifically, the purpose of the detection block 48 is to detect when the data lines  $sendat[15:0]$  are either all "0" or all "1". When either all "0" or all "1" is detected, the MATCH output goes to "1"; otherwise, the MATCH output remains at "0". The output logic 52 receives the MATCH output and generates a number of output data bits CMPOUT [15:0], Figure 5.

Roohparvar does not explicitly disclose "a logical OR operation having inputs coupled to the first and second match signals, the logical OR operation generating a true indication when one of the first or second match signals indicates a true state and a false indication otherwise". However, the implementation of logical OR operation, for comparing signals in a memory devices under test, is well known in the art. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a logical OR operation in the apparatus of Roohparvar for the

purpose of detecting false indications, since logical OR operations are routinely used in logical comparison functions.

Roohparvar does not explicitly disclose "an output buffer circuit that either passes the predetermined bit or is in a high impedance state in response to the first or second match signals". In analogous art, Manning discloses a buffer driver circuit 128, Figure 2, where if data read from a location in the banks 80a-80h does not match the data written to the location, the driver circuit 128 is driven to a tri-state condition. In the tri-state condition, the driver circuit 128 presents high impedance, floating output to the data bus 130. A test head 111 indicates the tri-state condition to test circuitry 113 that identify the erroneous data. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the output logic 52 of Roohparvar by incorporating a buffer driver circuit, which presents a high impedance, floating output to the data bus in response to a MATCH output signal as taught by Manning, so as to identify the erroneous data to a test circuitry.

Regarding Claims 21, Roohparvar discloses an electronic system, Figures 1, 2, comprising a processor (Figure 1, a memory chip tester 22) coupled to a memory chip 20 and also as shown in Figure 2 coupled to the memory chips 24, 26, 28, 30. The memory device having an output data compression apparatus, such as a pattern recognition block 40 in memory chips 24, 26, 28, 30, which receives the data sendat[15:0] from the sense amplifiers 34 and compress that data down to 4 bits, Figures 2, 4, 5, comprising:

a first circuit and a second circuit corresponding to detection block 48 in the pattern recognition block 40 for detecting patterns all "0" or all "1"; among the data bits sendat[15:0], i.e., detect patterns in which the data bits sendat[15:0] are arranged. Specifically, the purpose of the detection block 48 is to detect when the data lines sendat[15:0] are either all "0" or all "1". When either all "0" or all "1" is detected, the MATCH output goes to "1"; otherwise, the MATCH output remains at "0". The output logic 52 receives the MATCH output and generates a number of output data bits CMPOUT [15:0], Figure 5.

Roohparvar does not explicitly disclose "an output buffer circuit that either passes the predetermined bit or is in a high impedance state in response to the first or second match signals". In analogous art, Manning discloses a buffer driver circuit 128, Figure 2, where if data read from a location in the banks 80a-80h does not match the data written to the location, the driver circuit 128 is driven to a tri-state condition. In the tri-state condition, the driver circuit 128 presents high impedance, floating output to the data bus 130. A test head 111 indicates the tri-state condition to test circuitry 113 that identify the erroneous data. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the output logic 52 of Roohparvar by incorporating a buffer driver circuit, which presents a high impedance, floating output to the data bus in response to a MATCH output signal as taught by Manning, so as to identify the erroneous data to a test circuitry.

Regarding Claims 25, 26, Roohparvar substantially discloses the claimed invention as applied to claim 23, above. However, Roohparvar does not explicitly

disclose, "repairing the error condition and repairing each word". In analogous art, Manning discloses a test system, which monitors the data bus and identifies memory devices having defective rows or columns, which then can then be replaced by redundant rows or columns., See Summary of the Invention. Also, a test head 180 (Figure 3) monitors the data bus 130, and responsive to the tri-state output, registers the data as invalid. Additional test circuitry 182 receives the information from the test head 180 and indicates that the corresponding four columns include a defective column. The defective four columns can then be replaced by a set of four redundant columns.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to repair a defect in the device of Roohparvar by substituting a redundant row or column for the defective row or column as taught by Manning, so as to maximize the storage use of the memory device.

### ***Allowable Subject Matter***

Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 14-17, 22 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention for a bit match circuit including the structural limitations as recited in the independent claim 14.

Also, regarding independent claim 22, the prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious, "a plurality of propagation repeater circuits that regenerate the first and second match signals, a first propagation repeater circuit coupled between a predetermined number of the first series of bit match circuits and a second propagation repeater circuit coupled between a predetermined number of the second series of bit match circuits".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decayd can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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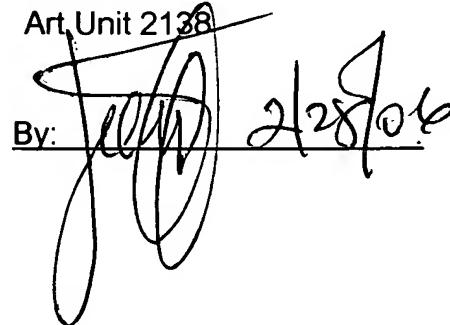
Date: 28 February 2006  
Office Action: Non-Final Rejection

JAMES C KERVEROS

Examiner

Art. Unit 2138

By:



2/28/06